AK Tech Training and Placements

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ASIC Implementation of Distributed Arithmetic Based FIR Filter using R...

This project presents an efficient implementation of memory less distributed arithmetic (MLDA) architecture in finite impulse response filter with residual number system. The input data and filter coefficients of MLDA are in residue number form and the output data from MLDA is converted into binary form using Chinese remainder theorem. In addition, compressor adders are used to reduce the area. For real time validation, the proposed design has been simulated and synthesized using Xilinx ISE 14.7.

Domain: Front End Domains / DSP Core
Technology: VLSI