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Anti-PVT-Variation Low-Power Time-to-Digital Converter Design using 90...

In this project, a Process, Voltage, Temperature (PVT) variation insensitive TDC featured with a PVT detector is proposed. Recently a lot of research has been carried out on Time to digital converters. TDC has many applications such as time of flight, radar ranging, and particle lifetime measurement. In TDC, high performance at different PVT corners is needed because it is used in wide range of applications such as ADCs, all-digital PLL, digital converters. The PVT detector takes advantage of another delay line with optimized locking conditions to differentiate PVT corners. The proposed TDC is physically realized using a 90nm CMOS process. The proposed TDC is physically realized using a 90-nm CMOS process in Cadence Virtuoso

Domain: Back End Domains / Cadence EDA
Technology: VLSI