AK Tech Training and Placements

Transform Dreams into Reality

A High-Performance Multiply-Accumulate Unit by Integrating Additions and Accumulations into Partial Product Reduction Process

In this project, we propose a low-power high-speed pipelined MAC architecture. Carry propagation of additions consume more power and large path-delay, to resolve this problem we introduce a proposed method. In this we integrate a part of additions into a partial product reduction process. Until the PPR process of next multiplication, addition and accumulation of MSB bits are not performed. To correctly contrast with surplus in the PPR process, a small size adder is designed to accumulate the total number of carries. Resemble with traditional methods proposed method significantly reduce the power consumption and circuit area. The effectiveness of the proposed method is designed using Xilinx ISE 14.7/Xilinx Vivado software.

Domain: Front End Domains / DSP Core
Technology: VLSI