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Transform Dreams into Reality

A novel phase-locked loop for mitigating the subsequent commutation failures of LCC-HVDC systems

Main objective of this project is to reduce the fluctuation of PLL's frequency during AC faults. And the estimated frequency is fixed when the fault is detected by a fault detector In this project, AC fault ride-through and support capability of Line Commutated Converter Based High Voltage Direct Current (LCC-HVDC) is proposed which have significant influence on the safe operation of power system. The ability of Phase Locked Loop (PLL) to synchronize with the voltage phase under AC faults would affect the recovery performance of LCC-HVDC systems. analyzes the influence of the conventional PLL on the Subsequent Commutation Failure (SCF) of LCC-HVDC systems and points out that the conventional PLL has some problems such as slow dynamic response, significant frequency fluctuation, and coupling of phase and frequency detection under fault conditions. A novel PLL is proposed to address the problems. Cascade delayed signal cancellation operators are combined with a mathematical filter, forming a hybrid pre-filter to extract fundamental positive sequence voltage for the PLL. To reduce the fluctuation of PLL's frequency during AC faults, the estimated frequency is fixed when the fault is detected by a fault detector. As a consequence, the decoupling between phase detection and frequency detection is realized, and the proposed PLL's dynamic response performance is enhanced. Simulation results show that the proposed PLL can provide accurate phase reference for the DC control system and reduce the probability of SCFs of LCC-HVDC system.

Domain: Power Systems _ HVDC
Technology: Electrical