# 8-Bit ALU Design using m-GDI Technique

In this project, an 8-bit Arithmetic Logic Unit (ALU) using Gate Diffusion Input (GDI) technique is proposed. Implementing the GDI technique in designing the ALU requires less number of transistors which result in reduced chip-area and power consumption – two of the most important parameters in digital VLSI design. In this design, 3T XOR is used in the full adder. Moreover, a novel 1-to-8 de multiplexer circuit has been used in the design as well. By using this method, we can reduce the power consumption in ALU design

**Domain:** Back End Domains / Transistor Logic
**Technology:** VLSI