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32-Bit Mac Unit Using Vedic Multiplier and Carry Save Adder

In this project The Multiply-Accumulate Unit (MAC) is an integral computational component of all Digital Signal Processing (DSP) architectures and thus has a significant impact on their speed and power dissipation and area overhead. To reduce the delay and area consumption the adders and multipliers are replaced with efficient adder and multiplier thereby implementing an efficient MAC unit. In this paper, an efficient and high performance MAC unit is implemented using carry save adder and Vedic multiplier for 32 bit operands. The proposed MAC unit has better area and delay compared to the existing MAC unit.

Domain: Front End Domains / Arithmetic Core
Technology: VLSI